PATENT ABSTRACTS OF JAPAN

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(71) Applicant : **TOSHIBA CORP**

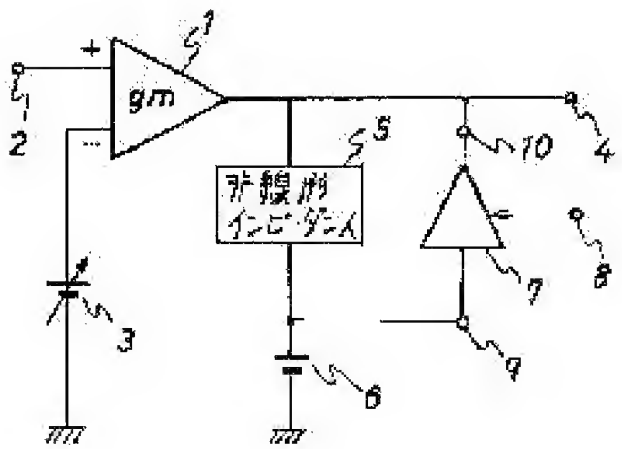
(72)Inventor : **KAWAGUCHI TOSHIHARU**

(54) GAMMA OFFSET ADJUSTMENT CIRCUIT

(57)Abstract:

PURPOSE: To adequately execute gamma correction to an input signal by providing a buffer circuit with a control terminal capable of fixing gamma corrected output to a reference DC level determined in an IC at optional timing.

CONSTITUTION: The buffer circuit 7 to be controlled by a control signal inputted to its control terminal 8 is connected in parallel with non-linear impedance 5. The input 9 of the buffer circuit 7 is connected to the junction point of the non-linear impedance 5 and reference power supply 6, and the output 10 of it is connected to an output terminal 4. Thus, the difference of output DC levels at the time when this circuit is operated and at the time when this circuit is not operated for certain fixed input level is read, and by adjusting this level difference so as to set it optionally, relation between a gamma correction curve and an input DC level can be determined adequately. Thus, the gamma correction can be executed to the input signal through very simple configuration.



* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the gamma offset adjustment circuit which sets up the input-reference DC levels of a video signal correctly to the gamma correction curve of a gamma correction circuit, for example in the video signal processing circuit of liquid crystal TV.
[0002]
[Description of the Prior Art]Drawing 7 shows the conventional gamma correction circuit. While this circuit connects the input terminal 2 to noninverting input + of the current output amplifier 1, connecting the input-reference power supply 3 to inversion input - and connecting the output terminal 4 to an output, one end of the nonlinear impedance 5 was connected and the other end of the nonlinear impedance 5 is connected to the reference supply 6.
[0003]Drawing 8 shows the concrete composition of the nonlinear impedance 5 of drawing 7. Each base of transistor Q9 and Q10, a collector, besides the end of the resistance R5 are connected to the output 4 side of the current output amplifier 1. The emitter of the transistor Q9 connects the emitter of the transistor Q10 to the anode of the reference supply 11 via the resistance R7 at the negative electrode of the reference supply 11, and the anode of the reference supply 12 via the resistance R6, respectively. The other end of the resistance R5 is connected to the negative electrode and the reference electrode 6 of the reference supply 12.
[0004]The input-output behavioral characteristics of the circuit shown in drawing 7 have a gamma correction curve shown in drawing 9. For example, if you would like to take the pedestal level of the video signal of the input terminal 2 at the starting point of a gamma correction curve, the DC levels of the input terminal 2 or the DC levels of the input-reference potential 3 are adjusted, and desired DC levels should just be obtained with the output terminal 4.
[0005]However, since the reference potential of a gamma correction curve differs in this method for every IC, and there is also output offset current of the current output amplifier 1 and the starting point of a gamma correction curve cannot be correctly known with an output when it is going to constitute the above-mentioned circuit within IC, exact adjustment cannot be performed, either. How to perform a pedestal clamp in an input is considered as a way stage of this adjustment. However, since it may be changing with direct-current transmission amendments etc. according to the signal level, the pedestal level of a actual video signal is not effective when such a signal is inputted.

[0006]
[Problem(s) to be Solved by the Invention]Since the relative position of the input level to the reference potential in IC did not understand the above-mentioned conventional gamma offset adjustment circuit when a pedestal clamping circuit is not used for an input, there was a problem that it was difficult to double with a desired position to a gamma correction curve.
[0007]An object of this invention is to provide the circuit which can double input DC levels with a desired position correctly to a gamma correction curve, even if there is no pedestal clamping circuit of an input.
[0008]
[Means for Solving the Problem]This invention provides a buffer circuit with a control terminal which can fix a gamma correction output to a reference DC level defined within IC to arbitrary timing.
[0009]
[Function]The relation between that of a gamma correction curve and input DC levels can be appropriately defined by adjusting so that the output DC-levels difference at the time of not making it operate with the time of operating this circuit to a certain fixed input level may be read and this level difference may be arbitrarily set up by the above-mentioned means.
[0010]
[Example]Hereafter, with reference to drawings, it explains in detail per example of this invention. Drawing 1 shows - example of this invention, gives the same numerals to drawing 7 and identical parts, and explains them focusing on a portion different here.
[0011]In drawing 1, this circuit is a different portion from drawing 7 in that the buffer circuit 7 controlled by the control signal inputted into the control terminal 8 in parallel with the nonlinear impedance 5 was connected. The buffer circuit 7 connects the input 9 at the node of the nonlinear impedance 5 and the reference supply 6, and connects the output 10 to the output terminal 4.
[0012]Drawing 2 shows the buffer circuit 7 of drawing 1 concretely. That is, the transistor Q1, Q2, Q3, and currant mirror CM1 constitute an operational amplifier. It connects with the nonlinear impedance 5 and the reference supply 6 of drawing 1 via the input 9 of the buffer circuit 7, and the base of the transistor Q1 used as the noninverting input of an operational amplifier connects the output of an operational amplifier to the output terminal 4. The current source of the operational amplifier which comprised the transistor Q4, Q5, the resistance R1, and R2 connects the transistor Q4 used as a current control input, and the base of Q5 to the control terminal 8.
[0013]If this buffer circuit 7 sends collector current through the transistor Q4 and Q5 by control of the control terminal 8, even if there is output offset of the current output amplifier 1 of drawing 1, the potential of the output terminal 4 will become equal to the potential of the input 9.
[0014]In drawing 1, if a control pulse like drawing 3 (b) turned on during [the] the pedestal is given to the control terminal 8 when a video signal like drawing 3 (a) is outputted to the output terminal 4, an output wave [like drawing 3 (c)] whose output terminal 4 is will be obtained. When a control pulse is ON, it means that the reference potential 6 of drawing 1 was inserted in the output as for this. Then, if the amplitude of the reference potential inserted in the output terminal 5 is adjusted, input signal DC levels can be appropriately set up to a gamma correction curve. What is necessary is just to adjust incidentally, to set the pedestal of an input signal by the starting point of a gamma correction curve so that a level difference may not come out, even if it inserts a reference potential.

[0015]In the above-mentioned example, since the input conversion DC offset produced with comparatively easy composition in a gamma correction circuit can be investigated easily, input DC levels can be set up the optimal.
[0016]Drawing 4 shows other examples of this invention. While this example connects conversely input and output of the buffer circuit 7 in drawing 1, It connects via the resistance R3 at the node of the nonlinear impedance 5 and the reference supply 6 from the output 10 side of the buffer circuit 7 which carried out multiple connection, and input and output of the buffer circuit 7 are supplied to the differential amplifier amplifier 10, and the output 10 is connected to the output terminal 4.
[0017]This example comes to show the output wave of the current output amplifier 1 to drawing 5 (a). When the buffer circuit 7 becomes active by the control pulse from the control terminal 8, this output becomes like drawing 5 (b). As a result, with the differential amplifier amplifier 10, the wave-like level of (a) and (b) is subtracted, and a final output comes to be shown in drawing 5 (c). In this example, since the input of the buffer circuit 7 is connected to the signal path, it is effective in the ability of the influence of f ****** by this to be disregarded, and will become very advantageous to broadband-izing.
[0018]The composition in particular of the buffer circuit 7 of the example described here is not limited to drawing 2. For example, it may be the same operational amplifier as drawing 2, and a switching circuit as stopped if the function can be suspended by OFF of a current source, etc., and shown in drawing 6 may be sufficient. The circuit of drawing 6 is connected to the collector of the transistor Q8 while it carries out interconnection of the transistor Q6 and the base of Q7, The collector of the transistor Q6 and the emitter of Q7 were connected to the input 9, the emitter of the transistor Q6 and the collector of Q7 were connected to the output terminal 4, the emitter of the transistor Q8 was grounded via the resistance R4, and the base is connected to the control terminal 8.
[0019]If this circuit sends the collector current of the transistor Q8 by control of the control terminal 8, the transistor Q6 and Q7 go into SACHU ration mode, and the impedance between the switch input 9 and the output terminal 4 will become low, and will flow through them. On the other hand, if the transistor Q8 is made to cut off, it will be in an open condition between the switch input 9 and the output terminal 4. In short, the DC levels of the output terminal 4 should just become abbreviated same electric potential to the DC levels of the input 9 according to the state of a control input equivalent.
[0020]In this explanation, although reference level was doubled with the suitable position to the pedestal level of a video signal, especially even if it is not pedestal level in particular, it does not interfere.
[0021]
[Effect of the Invention]As explained above, according to the gamma offset adjustment circuit of this invention, it is effective in the ability to perform a gamma correction appropriately to an input signal with very easy composition.

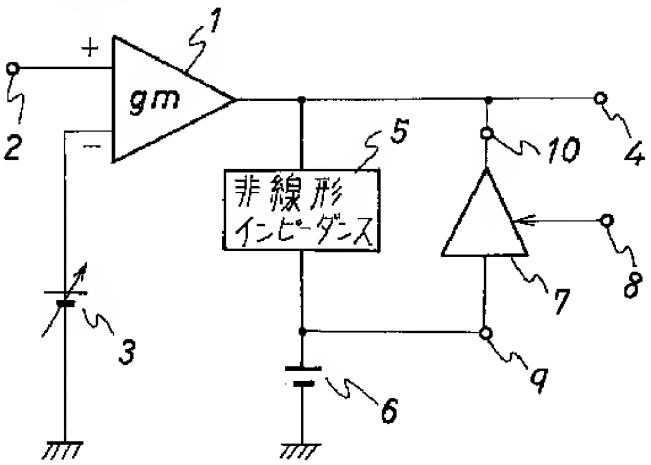
CLAIMS

[Claim(s)]
[Claim 1]A gamma offset adjustment circuit comprising:
An input terminal which inputs a video signal.
A current conversion circuit which changes into current an input signal inputted into the above-mentioned input terminal.
An output circuit linked to an output of the above-mentioned current conversion circuit.
A means to set an output level of the above-mentioned output terminal as the above-mentioned output reference potential only when multiple connection is carried out to nonlinear impedance connected between output reference potential, and the above-mentioned output reference potential and the above-mentioned output terminal, and the above-mentioned nonlinear impedance and a control signal is inputted.

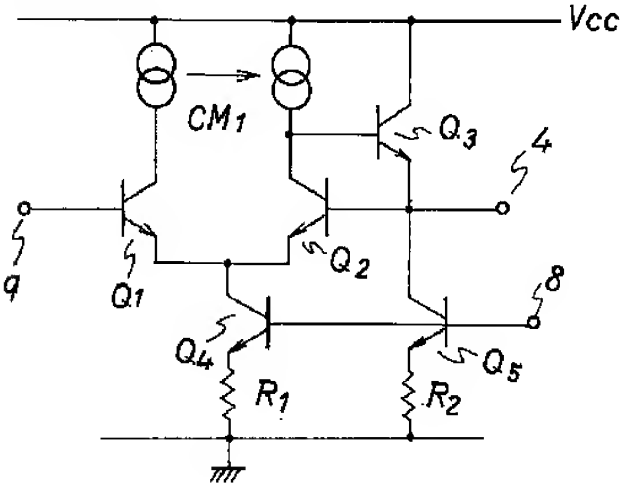
[Claim 2]A gamma offset adjustment circuit comprising:
An input terminal which inputs a video signal.
A current conversion circuit which changes into current an input signal inputted into the above-mentioned input terminal.
An output circuit linked to an output of the above-mentioned current conversion circuit.
Nonlinear impedance connected between output reference potential, and the above-mentioned output reference potential and the above-mentioned output terminal, Differential amplifier which connected the 1st input to the above-mentioned current conversion circuit, and connected the 2nd input via resistance from the above-mentioned output reference potential, A means to set a level of the 1st input of the above-mentioned differential amplifier as a level of the 2nd input of the above-mentioned differential amplifier only when it connects with an output terminal linked to an output of the above-mentioned differential amplifier between the 1st of the above-mentioned differential amplifier, and the 2nd input and a control signal is inputted.

DRAWINGS

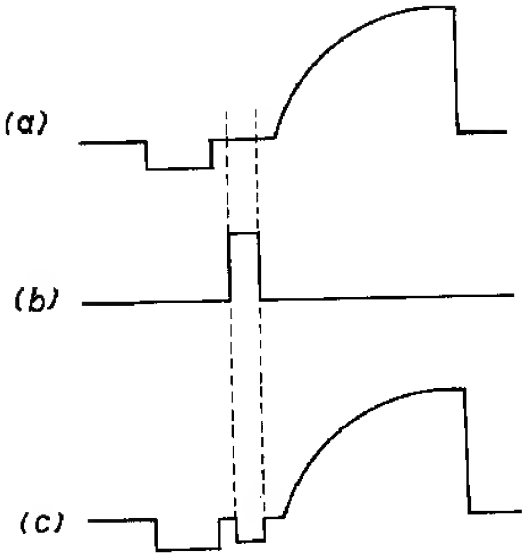
[Drawing 1]



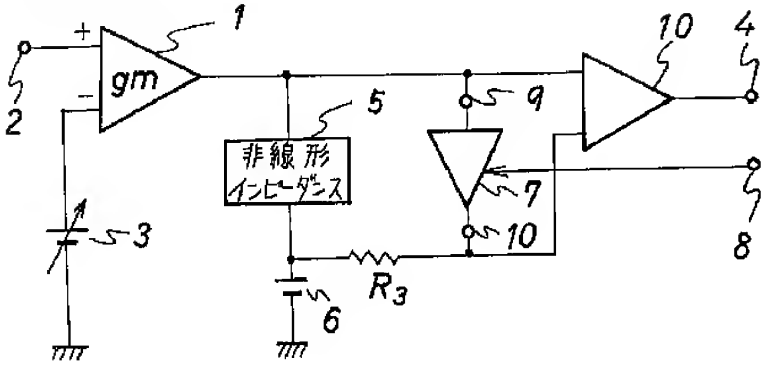
[Drawing 2]



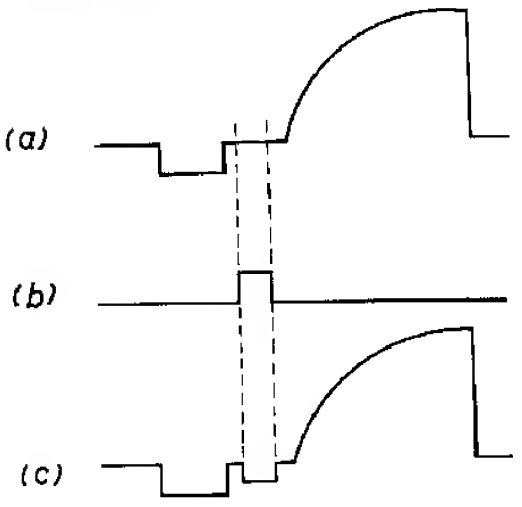
[Drawing 3]



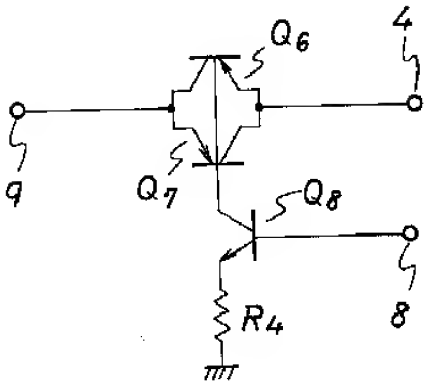
[Drawing 4]



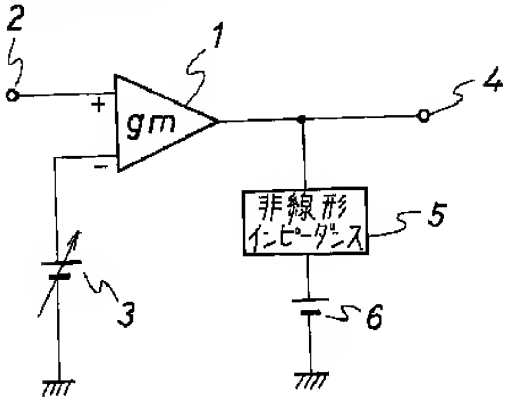
[Drawing 5]



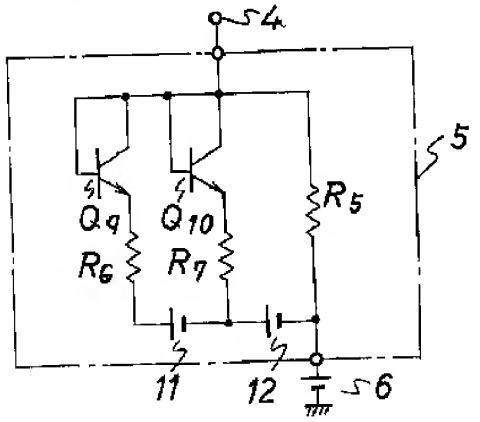
[Drawing 6]



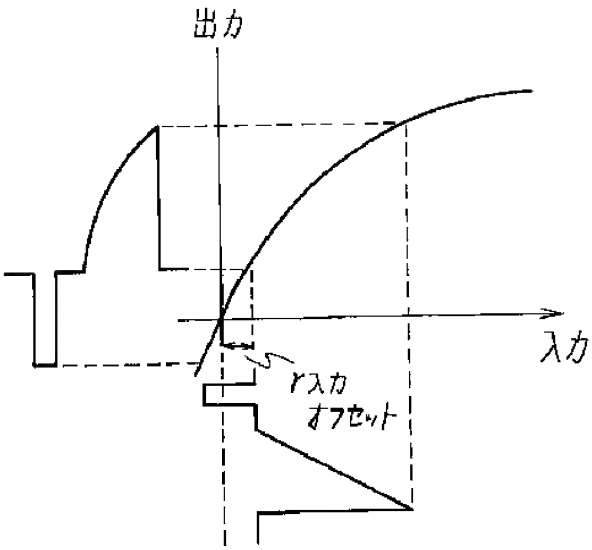
[Drawing 7]



[Drawing 8]



[Drawing 9]



[Translation done.]